UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/589,490	05/22/2007	Mitsunori Ishisaka	060471	8238

23850 7590 08/03/2010

KRATZ, QUINTOS & HANSON, LLP
1420 K Street, N.W.
4th Floor
WASHINGTON, DC 20005

EXAMINER	
CROWELL, ANNA M	
ART UNIT	**PAPER NUMBER**
1716	

MAIL DATE	DELIVERY MODE
08/03/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/589,490	ISHISAKA ET AL.	
	Examiner	Art Unit	
	Michelle Crowell	1716	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-5* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *08-15-06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5 are rejected under 35 U.S.C. 102(a) as being anticipated by Kasanami et al. (WO 2004/095560).

3. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasanami et al. (U.S. 2006/0151117).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Note. For purposes of examination, Kasanami et al. (U.S. 2006/0151117) will be used as the English translation for Kasanami et al. (WO 2004/095560).

Referring to Figures 3-5 and paragraphs [0051]-[0061], Kasanami et al. discloses a semiconductor manufacturing device comprising: a processing chamber 201 (Fig. 1, par. [0021])

including a susceptor 217 for supporting a substrate 200 (Fig. 5, par.[0050]), wherein the susceptor has a main body 1b containing a wall forming inside an electrode arranging space 8a substantially flat and parallel to the substrate and multiple pillars 9 joining the bottom and ceiling of the wall (Fig. 3, par.[0051]-[0052]); and a high-frequency electrode 2a installed with a gap between the electrode and at least the wall or at least the pillar 9 within the electrode arranging space 8a (Fig. 3 and (par.[0051-[0052]).

With respect to claim 2, the semiconductor manufacturing device of Kasanami et al. further includes wherein the distance from the high-frequency electrode 2a to the supporting surface 1a for supporting the substrate provided on the susceptor surface higher than the high-frequency electrode 2a, is set smaller than the distance from the high-frequency electrode 2a to the susceptor rear surface 1b lower than the high-frequency electrode (Figs. 3a and 5).

With respect to claim 3, the semiconductor manufacturing device of Kasanami et al. further includes wherein the electrode arranging space 8a is insulated from the atmosphere in the processing chamber and is connected to the atmosphere outside the processing chamber (par.[0054]-[0055]).

With respect to claim 4, a semiconductor manufacturing device further includes wherein the high-frequency electrode 2a is comprised of a plate formed with insertion holes where the pillars are inserted (Fig. 4).

With respect to claim 5, a method for manufacturing semiconductor devices comprising the steps of: supporting a substrate 200 on a susceptor 217 (Fig. 5, par.[0050]) installed in a processing chamber 201 (Fig. 1, par. [0021]), supplying and exhausting a process gas to and

from the processing chamber (par.[0022]), and performing plasma processing of the substrate (par.[0023]) by the susceptor having a main body containing a wall forming inside an electrode arranging space 8a substantially flat and parallel to the substrate and multiple pillars 9 joining the bottom and ceiling of the wall (Fig.3, par.[0051]-[0052]); and a high-frequency electrode 2a installed with a gap between the electrode and at least the wall or at least the pillar 9 within the electrode arranging space 8a (Fig. 3 and (par.[0051-[0052]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aruga et al. (U.S. 5,688,331) in view of Murakami (U.S. 5,462,603) and Arnold et al. (U.S. 5,423,971).

With respect to claims 1 and 5, referring to Figures 2 and 6 and column 4, line 1-column 6, line 50, Aruga et al. discloses a semiconductor manufacturing device comprising: a processing chamber 31 (Fig. 6) including a susceptor 39 for supporting a substrate (Figs. 1, 6, col. 4, lines 1-4) and a high-frequency electrode 41 installed in the susceptor 39.

Aruga et al fail to teach wherein the susceptor has a main body containing a wall forming inside an electrode arranging space substantially flat and parallel to the substrate and multiple pillars joining the bottom and ceiling of the wall; and a high-frequency electrode installed with a gap between the electrode and at least the wall or at least the pillar within the electrode arranging space.

Referring to Figures 1, 2, and column 3, line 60-column 6, line 46, Murakami teaches a semiconductor processing apparatus comprising a vacuum chamber 12 with a susceptor 13 having a main body 32 with a space formed inside it and which is substantially flat and parallel to the substrate and multiple pillars 40 joining the bottom 32a and ceiling 31 of the wall, and a heater 14 is installed inside the space (col. 4, line 62-col. 5, line 13). Murakami also teaches that the space inside the hollow cylindrical portion 33 (and thus the space inside the main body 32) is connected to atmosphere (as it is maintained at substantially the atmospheric pressure by passage of an inert gas), but is air-tightly segregated from the corrosive environment in the vacuum chamber 12. Murakami goes on to teach that in such an arrangement an inert gas is circulated (at atmospheric pressure) in the susceptor 13, 32, so as to prevent corrosion of the heater and the electrical feed lines, thus prolonging the life of the heater and the feeder lines, and ensures supply electrical power reliably to the heater (e.g. Figs. 1, 2 and col. 3, line 60 to col. 6, line 46). It would be obvious to form a space inside the susceptor's main body for locating the high

frequency electrode, which is substantially flat and parallel to the substrate and multiple pillars joining the bottom and ceiling of the wall, and the space is connected to the atmosphere for passage of an inert gas, to prolong the life of the high frequency electrode and ensure supply electrical power reliably to the high frequency electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form a space inside the susceptor for installing the high frequency electrode, which is substantially flat and parallel to the substrate and multiple pillars joining the bottom and ceiling of the wall, and the space is connected to the atmosphere as taught by Murakami in the apparatus of Aruga et al to prolong the life of the high frequency electrode and ensure reliable electrical supply to the high frequency electrode.

Aruga et al in view of Murakami fail to explicitly teach the high frequency electrode is installed with a gap between the electrode and at least the wall or at least the pillar within the electrode arranging space.

Referring to Figure 2 and column 4, line 25-column 5, line 8, Arnold et al teach semiconductor processing apparatus comprising a susceptor 52 formed with a space and a high frequency electrode 31 installed with a gap "c" between the electrode and the walls forming the space. Arnold et al further teach that gap "c" corresponds to dark space distance to prevent generation of spurious discharges. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to install the high frequency electrode with a gap between the electrode and the walls forming the space in the susceptor as taught by Arnold et al in the apparatus of Aruga et al in view of Murakami to prevent generation of spurious discharges.

With respect to claim 2, the semiconductor manufacturing device of Aruga et al. in view of Murakami and Arnold et al. further includes wherein the distance from the high-frequency electrode 14 (i.e. heater) to the supporting surface for supporting the substrate provided on the susceptor surface higher than the high-frequency electrode, is set smaller than the distance from the high-frequency electrode to the susceptor rear surface lower than the high-frequency electrode (Fig. 2 of Murakami).

With respect to claim 3, the semiconductor manufacturing device of Aruga et al. in view of Murakami and Arnold et al. further includes wherein the electrode arranging space is insulated from the atmosphere in the processing chamber and is connected to the atmosphere outside the processing chamber (discussed above in claim 1 and col. 6, lines 28-45 of Murakami).

With respect to claim 4, a semiconductor manufacturing device of Aruga et al. in view of Murakami and Arnold et al. further includes wherein the high-frequency electrode 14 is comprised of a plate formed with insertion holes where the pillars 40 are inserted (Fig. 2 of Murakami).

With respect to claim 5, a method for manufacturing semiconductor devices of Aruga et al. in view of Murakami and Arnold et al. as discussed above and further comprising the steps of: supplying and exhausting a process gas to and from the processing chamber (col. 6, lines 9-13, col. 5, lines 58-60 of Aruga et al.), and performing plasma processing of the substrate (col. 7, lines 5-8 of Aruga et al.).

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned

with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1 and 5 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 8 of copending Application No. 12/153,101 (U.S. 2008/0223524). Although the conflicting claims are not identical, they are not patentably distinct from each other because examined claims 1 and 5 are fully encompassed by claim 8 of copending application 12/153,101.

Referring to claim 8, Kasanami et al. discloses a semiconductor manufacturing device comprising: a processing chamber 201 including a susceptor 217 for supporting a substrate 200, wherein the susceptor has a main body containing a wall forming inside an electrode arranging space 8a substantially flat and parallel to the substrate and multiple pillars 9 joining the bottom and ceiling of the wall; and a high-frequency electrode 2a installed with a gap between the electrode and at least the wall or at least the pillar 9 within the electrode arranging space 8a.

With respect to claim 5, referring to claim 8, Kasanami et al. discloses a method for manufacturing semiconductor devices comprising the steps of: supporting a substrate 200 on a susceptor 217 installed in a processing chamber 20, supplying and exhausting a process gas to and from the processing chamber, and performing plasma processing of the substrate by the susceptor having a main body containing a wall forming inside an electrode arranging space 8a substantially flat and parallel to the substrate and multiple pillars 9 joining the bottom and ceiling

of the wall; and a high-frequency electrode 2a installed with a gap between the electrode and at least the wall or at least the pillar 9 within the electrode arranging space 8a.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Litman et al.'104, Barnes et al.'585, Kanno et al.'233, Shamouilian et al.'928, and Watanabe et al.'334 teach semiconductor manufacturing devices having an electrode within the susceptor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Crowell whose telephone number is (571)272-1432. The examiner can normally be reached on M-Th (9:30 -6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571) 272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Parviz Hassanzadeh/
Supervisory Patent Examiner, Art Unit 1716

/Michelle Crowell/
Examiner, Art Unit 1716